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Description

ALL-IN-ONE POLISHING PROCESS FOR A SEMICONDUCTOR WAFER

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an all-in-one polishing process for a semiconductor wafer, and more specifically, to a method of performing two chemical mechanical polishing (CMP) processes to respectively polish a top surface and an edge bevel surface of the semiconductor wafer, and performing a cleaning process and a drying process thereafter.

[0003] 2. Description of the Prior Art

[0004] Chemical mechanical polishing (CMP) is a method of polishing materials, such as a semiconductor wafer, to a high degree of planarity and uniformity. The process is used to planarize a semiconductor wafer prior to the fabrication of microelectronic circuitry thereon, and is also used to re-

move high-elevation features created during the fabrication of the microelectronic circuitry on the surface of the semiconductor wafer.

[0005] Please refer to Fig.1 and Fig.2, which respectively present a top view and a cross-sectional view of a semiconductor wafer 10 according to the prior art. As shown in Fig.1 and Fig.2, the semiconductor wafer 10 comprises a top surface 10a, an edge bevel surface 10b and a bottom surface 10c, and the edge bevel surface 10b comprises a front side bevel 10b1, a backside bevel 10b2 and an edge 10b3. The top surface 10a comprises at least a first material layer 12, comprising at least a semiconductor structure (not shown), such as a dual damascene structure or a capacitor structure, on the top surface 10a, and the edge bevel surface 10b comprises a second material layer 14, either spontaneously formed with the first material layer 12 or formed prior to the formation of the first material layer 12, needing to be completely removed due to the product specification. Either the first material layer 12 or the second material layer 14 comprises either a dielectric layer or a metal layer, and is formed by performing either a chemical vapor deposition (CVD) process or an electric copper plating (ECP) process. In the preferred embodi-

ment of the present invention, the first material layer 12 and the second material layer 14 are respectively composed of two different materials. Alternatively, the first material layer 12 and the second material layer 14 are composed of a same material. In addition, the edge 10b3 of the semiconductor wafer 10 comprises a notch 16 for locating the coordination of the semiconductor wafer 10 during the polishing and cleaning of the semiconductor wafer 10.

[0006] Please refer to Fig.3 of a schematic view of a chemical mechanical polishing device (CMP device) 20 according to the prior art. As shown in Fig.3, the CMP device comprises a polishing plate 22, a polishing pad 24 disposed on the polishing plate 22, a head 28 for pressing the semiconductor wafer 10 onto the polishing pad 24, a slurry supply tube 30, a cleaning solution supply tube 26 and a conditioner 32 for controlling the polishing pad 24 and removing flakes generated during polishing of the semiconductor wafer 10. The head 28comprises a holder (not shown) for containing the semiconductor wafer 10, the slurry supply tube 30 provides slurry on the semiconductor wafer during the polishing of the semiconductor wafer 10, and the cleaning solution supply tube 26 provides either a

cleaning solution (not shown) or deionized water (DI water, not shown), during the cleaning of the semiconductor wafer 10and the polishing pad 24.

[0007] The method of polishing and cleaning the semiconductor wafer 10 according to the prior art begins with adding the slurry on the top surface 10a of the semiconductor wafer 10. A CMP process is then performed by utilizing the polishing pad 24 of the CMP device to polishing portions of the first material layer 12 down to a first thickness based on the produce requirement, and the semiconductor wafer is sent to a buffing pad (not shown) softer than the polishing pad 24 thereafter. A buffing process, utilizing either the cleaning solution or DI wafer provided by the cleaning solution supply tube 26, is then performed to remove flakes of the first material layer 12 and residual slurry on the top surface 10a of the semiconductor wafer 10.

[0008] Finally, a chemical cleaning process and a drying process are performed to clean and dry the semiconductor wafer 10, as shown in Fig.4 of the cross-sectional view of the polished and cleaning semiconductor wafer 10.

[0009] However, as shown in Fig.4, the second material layer 14 needing to be completely removed remains on the edge

bevel surface 10b after portions of the first material layer 12 are removed down to the first thickness and the cleaning process is performed to cleaning the semiconductor wafer 10. Pealing of the remaining second material layer 14 frequently occurs in subsequent process due to thermal stress or other reasons, leading to the cracking of the second material layer 14. Flakes and particles of the second material layer 14 caused by the cracking thereof frequently fall on and therefore contaminate a top surface of another semiconductor wafer adjacent to the semiconductor wafer 10 during either a CVD process or the transportation of a batch of semiconductor wafers, making the performance of the product defective.

SUMMARY OF INVENTION

[0010] It is therefore a primary object of the present invention to provide an all-in-one polishing process for a semiconductor wafer so as to prevent a residual second material layer on the semiconductor in the method of polishing and cleaning a semiconductor wafer according to the prior art.

[0011] According to the claimed invention, the semiconductor wafer is positioned on a wafer stage of a chemical mechanical polishing (CMP) device and comprises a top sur-

face, a bottom surface and an edge bevel surface. The top surface comprises at least a first material layer, and the edge bevel surface comprises a second material layer. By utilizing a polishing pad to perform a surface CMP process, portions of the first material layer on the top surface is removed down to a first thickness. A rim CMP process is then performed to completely remove the second material layer on the edge bevel surface. A surface buffing process is performed by spraying either a cleaning solution or deionized water (DI water) on the semiconductor wafer thereafter to remove the slurry as well as the flakes of the second material layer. Finally, a chemical cleaning process is performed to clean the semiconductor wafer, and the semiconductor wafer is dried thereafter.

[0012] It is an advantage of the present invention against the prior art that the surface CMP and the rim CMP processes are performed to respectively polish the first material layer on the top surface down to the first thickness and completely remove the second material layer on the edge bevel surface 50b, and the CMP device employed comprises at least one cleaning solution supply tube and is considered an improved apparatus capable of performing not only the surface CMP process and the rim CMP pro-

cess but also a second cleaning process for cleaning the top surface and the chemical cleaning process. Therefore, the method of polishing the semiconductor wafer revealed in the present invention is called an all-in-one technology comprising the surface CMP process, the rim CMP process, the chemical cleaning process and the second cleaning process. In addition, the rim CMP process is employed to completely remove the second material layer. Contaminant caused by the pealed flakes of the residual second material layer due to thermal stress or other reasons in subsequent processes as revealed in the prior art is therefore prevented, assuring the performance of the product.

[0013] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the multiple figures and drawings.

Brief Description of Drawings

[0014] Fig.1 is a top view of a semiconductor wafer according to the prior art.

[0015] Fig.2 is a cross-sectional view of the semiconductor wafer according to the prior art.

[0016] Fig.3 is a schematic view of a chemical mechanical polish-

ing device (CMP device) according to the prior art.

[0017] Fig.4 is the cross-sectional view of the polished and cleaning semiconductor wafer according to the prior art.

[0018] Fig.5 is the top view of a semiconductor wafer according to the present invention.

[0019] Fig.6 is the cross-sectional view of a semiconductor wafer according to the present invention.

[0020] Fig.7 is the cross-sectional view of the semiconductor wafer after the surface CMP process and the surface cleaning process according to the present invention.

[0021] Fig.8 is the schematic view of a rim CMP device employed in the all-in-one polishing process according to the present invention.

[0022] Fig.9 is the schematic view of the rim CMP process of the all-in-one polishing process according to the present invention.

DETAILED DESCRIPTION

[0023] Please refer to Fig.5 and Fig.6, which respectively represent a top view and a cross-sectional view of a semiconductor wafer 50 according to the present invention. As shown in Fig.5 and Fig.6, the semiconductor wafer 50 comprises a top surface 50a, a edge bevel surface 50b located at the rim of the semiconductor wafer 50, and a

bottom surface 50c. The edge bevel surface 50b has a width of several millimeters and comprises a front side bevel 50b1, a backside bevel 50b2 and an edge 50b3. Normally, the edge bevel surface 50b can be employed for the alignment of the semiconductor wafer 50 to manufacturing machines during various semiconductor processes. The top surface 50a comprises at least a first material layer 52 formed on the top surface 50a, and the first material layer 52 comprises a semiconductor structure (not shown), such as a dual damascene structure or a capacitor structure. The edge bevel surface 50b comprises a second material layer 54, which is either spontaneously formed with the first material layer 52 or formed prior to the formation of the first material layer 52, needing to be completely removed due to the product specification. Either the first material layer 52 or the second material layer 54 comprises either a dielectric layer or a metal layer, and either the first material layer 52 or the second material layer 54 is formed by processes with full coverage, such as a chemical vapor deposition (CVD) process or an electric copper plating (ECP) process. In the preferred embodiment of the present invention, the first material layer 52 and the second material layer 54 are respectively com-

posed of two different materials. Alternatively, the first material layer 52 and the second material layer 54 are composed of a same material. In addition, the edge 50b3 of the semiconductor wafer 50 comprises a notch 56 for locating the coordination of the semiconductor wafer 50 during the polishing and cleaning of the semiconductor wafer 50.

[0024] After adding a first slurry (not shown) on the top surface 50a of the semiconductor wafer 50, a surface chemical mechanical polishing (surface CMP) process is performed to remove portions of the first material layer 52 on the top surface 50a down to a first thickness according to the specification requirement of the product. A first cleaning solution (not shown), comprising deionized water (DI water), is then sprayed onto the top surface 50a of the semiconductor wafer 50, and a surface cleaning process is performed to remove residual first slurry and flakes of the first material layer 52.

[0025] Please refer to fig.7 of the cross-sectional view of the semiconductor wafer 50 after the surface CMP process and the surface cleaning process are performed according to the present invention. As shown in Fig.7, the top surface 50a of the semiconductor wafer 50 turns to be a flat

surface after the surface CMP process and the surface cleaning process are performed. The steps and devices utilized for the performance of the surface CMP process and the surface cleaning process are similar to those revealed in the prior art, and are therefore neglected for simplicity of description.

[0026] Please refer to Fig.8 of a schematic view of a rim chemical mechanical polishing device (rim CMP device) 60 employed in the all-in-one polishing process for the semiconductor wafer 50 according to the present invention. As shown in Fig.8, the rim CMP device 60 comprises a wafer stage 62, a buffing pad 64, a notch pad 66, a plurality of rollers 68, at least one front side bevel pad 70, at least one backside bevel pad 72, at least one edge pad 74, at least one slurry supply tube 76 and at least one cleaning solution supply tube 78. The wafer stage 62 is employed for containing the semiconductor wafer 50, the notch pad 66 is employed for locating the coordination of the semiconductor wafer 50 on the wafer stage 62, and the rollers 68 are employed for fixing the semiconductor wafer 50 on the wafer stage 62. The slurry supply tube 76 provides a second slurry (not shown) on the semiconductor wafer 50 during the polishing of the second material layer 54, and

the cleaning solution supply tube 78 provides a second cleaning solution (not shown), comprising either chemicals or DI water, during the cleaning of the semiconductor wafer 50.

[0027] Please refer to Fig.9 of the schematic view of the rim CMP process of the all-in-one polishing process for the semiconductor wafer 50 according to the present invention. As shown in Fig.9, the second slurry provided by the slurry supply tube 76 is then added onto the edge bevel surface 50b of the semiconductor wafer 50, and the rim CMP process is performed thereafter to polish and completely remove portions of the second material layer 54 respectively on the front side bevel 50b1, the backside bevel 50b2 and the edge 50b3 by utilizing the front side bevel pad 70, the backside bevel pad 72 and the edge pad 74, respectively. In the preferred embodiment of the present invention, an angle between the semiconductor wafer 50 and either the front side bevel pad 70 or the backside bevel pad 72 ranges between 15 to 28 degrees during the rim CMP process due to the slopes of the front side bevel 50b1 and the backside bevel 50b2 to the semiconductor wafer 50. Simultaneously, a buffing polishing process is optionally performed on the top surface 50a by utilizing the buffing

pad 64 in order to achieve an excellent uniformity of the top surface 50a. A surface and edge bevel cleaning process, utilizing the cleaning solution provided by the cleaning solution supply tube 78, is then performed to clean the top surface 50a, the front side bevel 50b1, the backside bevel 50b2, the edge 50b3 and the surface of the semiconductor wafer, completely removing flakes of the second material layer 54 and residual portions of the second slurry on the top surface 50a, the front side bevel 50b1, the backside bevel 50b2, the edge 50b3 and the surface of the semiconductor wafer, as shown in Fig.9.

[0028] Finally, a chemical cleaning process and a drying process are performed to respectively remove residual slurry and dry the semiconductor wafer 50 at the end of the method revealed in the present invention.

[0029] In another embodiment of the present invention, the rim CMP process and the edge bevel cleaning process are alternatively performed on the edge bevel surface 50b of the semiconductor wafer 50 before the surface CMP process, the buffing polishing process and the surface cleaning process are performed on the top surface 50a of the semiconductor wafer 50, and the chemical cleaning process and the drying process are then performed to re-

spectively clean and dry the semiconductor wafer 50. The tools and steps utilized in the rim CMP process, the edge bevel cleaning process, the surface CMP process, the surface cleaning process and the drying process are similar to those in the preferred embodiment of the present invention and are neglected for simplicity of description.

[0030] In comparison with the prior art, the present invention utilizes the surface CMP and the rim CMP processes to respectively polish the first material layer 52 on the top surface 50a down to the first thickness and completely remove the second material layer 54 on the edge bevel surface 50b, and the CMP device 60 employed comprises the buffing pad 64 and is considered an improved apparatus capable of performing not only the surface CMP process and the rim CMP process but also the surface cleaning process and the edge bevel cleaning process without introducing additional manufacturing machines or processes that may increase production cost. Therefore, the method of polishing the semiconductor wafer 50 revealed in the present invention is called an all-in-one technology comprising the surface CMP process, the rim CMP process, the surface cleaning process and the edge bevel cleaning process. In addition, the rim CMP process is em-

ployed to completely remove the second material layer 54. Contaminant caused by the pealed flakes of the residual second material layer 14 due to thermal stress or other reasons in subsequent processes as revealed in the prior art is therefore prevented because of the improved uniformity of the edge bevel surface 50b achieved by the rim CMP process and the edge bevel cleaning process revealed in the present invention, assuring the performance of the product.

[0031] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bound of the appended claims.